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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/181,253	10/28/1998	GREGORY MICHAEL KAROL	FOM-143.01.	9665

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EXAMINER
KUMAR, PANKAJ

ART UNIT	PAPER NUMBER
2631	8

DATE MAILED: 03/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/181,253	KAROL, GREGORY MICHAEL	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/10/2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 1/10/2003 have been fully considered but they are not persuasive.

2. The office respectfully traverses applicant's argument that Bedrosian does not teach selective coupling. Bedrosian in fig. 9B teaches that the output of VCO is selectively coupled with the AND gate since the AND gate selects an output based on the VCO output and a D-flip-flop output.

3. The office respectfully traverses applicant's argument that Bedrosian does not teach selective coupling is controlled by said clock detection circuit output. Selective coupling of the feed-forward and feedback filters is controlled, via other components from fig. 9A and 9B, by said clock detection circuit output.

4. Bedrosian teaches that figs. 9A and 9B are explained with respect to other figures. One of these other figures is figure 2 which shows multiplexers 202, feedforward with the clock and sync outputs being fed forward through 216 whose output goes to 206 whose output goes to 208, feedback with the output clock feeding back to 206 and 216 whose output goes to 208 and 204, respectively.

5. Claim 15 has been amended and accordingly, a new ground of rejection has been set forth for claim 15.

6. The office respectfully traverses applicant's arguments for claims 16-20 when the applicant says that Richards does not teach detecting a clock source failure and adjusting a time constant. Based on the quote cited in the prior action, Richards teaches clock source failure with

clock drift and Richards teaches adjusting a time constant with adjusting time constant J or user determined factor m which sets the time constant. Applicant's claim does not say that a time constant cannot be determined with a user determined factor.

Response to Amendment

1. Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

3. A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Fazakerly et al. USPN 4208635.

5. As per claim 15, a circuit comprising: a clock source (Fazakerly fig. 1: reference frequency); a PLL circuit having said clock source as its input (Fazakerly fig. 1: 10, 12, 14); a detection circuit coupled to said clock source (Fazakerly fig. 1: output of 10) and having an output representative of a presence of said clock source (Fazakerly fig. 1: output of 10 is representative of its input); and a feedforward correction circuit (Fazakerly fig. 2: 34, 36) coupled to said output of said detection circuit (Fazakerly fig. 2: Vout) and to a feedback loop of said PLL (Fazakerly fig. 2: 46, 51; col. 3 line 50 to col. 4 line 12).

6. Claims 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Richards et al. USPN 6,178,207.

7. See prior action for details.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bedrosian USPN 5,740,211.

10. As per claim 1, a clock circuit comprising: first (Bedrosian fig. 9A: side 0 monitor output) and second clock sources (Bedrosian fig. 9A: side 1 monitor output); a multiplexer having a first input (Bedrosian fig. 9A: CLK MUX top input) coupled to the first clock source, a second input (Bedrosian fig. 9A: CLK MUX bottom input) coupled to the second clock source (Bedrosian col. 4 fourth paragraph "(12) The hitless switch device 130 has an input multiplexer 202 which is connected to clock distribution circuits 120, 121 and is capable of receiving a side 0 set of clock and sync signals, and a side 1 set of clock and sync signals therefrom. Input multiplexer 202 selects between these sets of clock and sync signals from sides 0 or side 1. The switching selection is controlled either by input failure monitors or by a manual command (not shown)."), and an output selectively couplable to said first and second inputs (Bedrosian fig. 9A: bottom output of CLK MUX into flip flop in which one of the inputs is a select into the D input

of the flip flop); a clock detection circuit having an output representing a presence of said first clock source (Bedrosian fig. 9A: bottom NOR gate); said multiplexer having a selection input coupled to said clock detection circuit output (Bedrosian fig. 9A: NOR gate coupled to CLK MUX via flip flop) such that said multiplexer selects said first clock source as its output when said first clock source is present (Bedrosian fig. 9A: system will force 0 or force 1 depending on whether 0 or 1 is present); a phase-locked loop circuit ("PLL") (Bedrosian fig. 9B) having an input coupled to said multiplexer output (Bedrosian fig. 9A output from CLK MUX goes into fig. 9B top input) and a frequency output (Bedrosian fig. 9A output from SYNC MUX goes into fig. 9B bottom input), said PLL including a feedback filter circuit (Bedrosian fig. 9B: LPF 2nd order and VCO); and feedforward circuitry (Bedrosian fig. 9B: number of locations for example – top input going through latch, inverter and AND gate circuits in order to reach phase compare circuit while top input also going through middle and bottom latches which eventually affect the D latch towards the middle left of the diagram whose output is eventually fed into the phase comparator) coupled to said feedback filter circuit (Bedrosian fig. 9B: phase comparator is coupled to LPF) and coupled to said clock detection circuit output (Bedrosian fig. 9B: latches 0011, 0100, and two 0001 are clock enabled and thus they are detecting clocks), said feedforward circuitry selectively coupling at least one circuit element (Bedrosian fig. 9B: output of VCO is selectively coupled with the AND gate since the AND gate selects an output based on the VCO output and a D-flip-flop output) to said feedback filter circuit (Bedrosian fig. 9B: LPF and VCO), wherein said selective coupling (rejected under 112) is controlled by said clock detection circuit output (Bedrosian does not teach this. Instead, Bedrosian teaches selective coupling of the feed-forward and feedback filters is controlled, via other components from fig.

9A and 9B, by said clock detection circuit output as discussed with fig. 9A. It would have been obvious to one skilled in the art at the time of the invention to modify Bedrosian to teach selective coupling controlled by said clock detection circuit output since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.).

11. As per claim 2, the circuit of claim 1, where said feedforward circuitry includes a switch controlled by said clock detection circuit output and performing said selective coupling (Bedrosian fig. 9B: the second input into the ET phase compare whose output eventually goes into the LPF is derived via a clock through the AND gate inputting into the ET phase compare. AND gate is working as a switch since its output will only switch high when both of its inputs are switched high. Selective coupling is occurring since the clock is selected (select 0/1) prior to these steps).

12. As per claim 3, the circuit of claim 2, wherein said switch comprises a transistor (Bedrosian fig. 9A: inherent for the flip flop to have transistors).

13. As per claim 4, the circuit of claim 2, wherein said at least one circuit element includes a resistor (Bedrosian fig. 2: 206 "pulse blocker").

14. As per claim 5, the circuit of claim 4, wherein said at least one circuit element includes a capacitor in parallel with said resistor (not in Bedrosian; however, the selection of known material based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over that prior art (In re Leshin, 125 USPQ 416).).

15. As per claim 6, the circuit of claim 2, wherein said feedforward circuitry includes at least one of a resistor and a capacitor in parallel with said switch (not in Bedrosian; however, the

selection of known material based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over that prior art (In re Leshin, 125 USPQ 416).).

16. As per claim 7, the circuit of claim 2, further including a bias circuit coupling said clock detection circuit output to said switch (Bedrosian fig. 9B: the D latch towards the middle left of the diagram is the bias circuit coupling the clock output to the AND gate which is essentially functioning as a switch).

17. As per claim 8, the circuit of claim 7, wherein said bias network includes a resistor based voltage divider. (not in Bedrosian; however, the selection of known material based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over that prior art (In re Leshin, 125 USPQ 416).).

18. As per claim 9, the circuit of claim 8, further including a zener diode in parallel with at least one resistor of said resistor base voltage divider. (not in Bedrosian; however, the selection of known material based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over that prior art (In re Leshin, 125 USPQ 416).).

19. As per claim 10, the circuit of claim 1, wherein said first clock source (Bedrosian fig. 9A: Side 0) is received from another clock circuit within a common system (Bedrosian fig. 9A: received by monitor for clk mux as well as monitor for sync mux).

20. As per claim 11, the circuit of claim 10, wherein said first clock source is received over a bus. (Bedrosian fig. 9A: inputs into monitors are indicated as buses since a width of 2 is indicated for the inputs to the monitors)

21. As per claim 12, the circuit of claim 11, wherein said second clock source comprises a local oscillator. (inherent for a clock source to comprise a local oscillator since a clock source is itself oscillating)

22. As per claim 13, the circuit of claim 12, wherein said second clock source (Bedrosian fig. 9A: Side 1) is provided to said bus (Bedrosian fig. 9A: inputs into the monitor is indicated as a bus since a width of 2 is indicated).

23. The rejection of claim 14 is discussed in respect to the discussion of claim 1.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

PK
March 18, 2003